wherein at least one of said plurality of electrodes and at least one of said plurality of leads are electrically connected; and

wherein on said substrate in a region including at least a part of a region opposing said semiconductor chip, a film is formed with a lower adhesion to said adhesion than a base material of said substrate, the film formed in such a shape as to avoid the electrodes.

REMARKS

Claims 1-22 are pending. By this Amendment, claims 11 and 20 are canceled and claims 1 and 12 are amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. 1.121(b)(1)(iii)) and claim (37 C.F.R. 1.121(c)(1)(ii)).

I. THE SPECIFICATION SATISFIES ALL FORMAL REQUIREMENTS

The Office Action objects to the specification because the specification does not include reference sign 132 of Fig. 9. The Examiner is directed to page 24, line 4 of the specification for a disclosure of Reference sign 132.

The Office Action also objects to the specification because Reference No. "12" should be --14-- on page 12, line 15 of the specification. Accordingly, Reference symbol "14" has been changed to --12--.

Withdrawal of the objection to the specification is respectfully requested.

II. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claim 12 under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,175,151 B1 to Hashimoto; claims 1, 2, 6-13 and 15-22 are rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,731,631 to Yama et al.; and claims 3-5

and 14 are rejected under 35 U.S.C. §103(a) as unpatentable over Yama et al. in view of Japanese Patent A-10112475. These rejections are respectfully traversed.

Hashimoto does not constitute prior art. The effective prior art date for Hashimoto is February 18, 1999. However, the present application claims priority from Japanese Application 10-326184 filed October 30, 1998. Thus, Hashimoto does not constitute prior art, and withdrawal of the rejection of claim 12 under 35 U.S.C. §102(e) is respectfully requested.

Yama does not disclose on a substrate in a region including at least a part of a region opposing the semiconductor chip, a film is formed with a lower adhesion to the adhesive than a base material of the substrate the film formed in such a shape as to avoid the electrodes, as claimed in claims 1 and 12.

Instead, Yama discloses lands on which electrodes of the semiconductor chip are positioned. Additionally, Yama discloses a substrate 3 and electrodes 16 and 2 along with leads 7. Lands 5 serve as electrodes and are formed on the surface of the substrate 3 and are electrically connected to the electrodes 4 through signal lines formed within the substrate 3. Conductive resin 19 electrically and mechanically connects together the electrode pad 16 and the lands 17 for internal bumps together.

Thus, there is no teaching, disclosures or even suggestions in Yama for having on the substrate in a region including at least a part of a region opposing said semiconductor chip, a film being formed with a lower adhesion to the adhesive than a base material of said substrate and the film formed in such a shape as to avoid the electrodes, as claimed in claims 1 and 12.

Because Yama does not disclose the features of claims 1 and 12, it cannot provide advantages of the claimed invention. For example, Yama does not provide the advantage of more easily dispersing holes and voids on the film surface and are reduced in size to a

tolerable level. Thus, as a result, the accumulation of moisture in voids and holes can be prevented, and a semiconductor device of high reliability can be manufactured.

However, the structure of Yama is completely devoid of these advantages. The fact that the structure of Yama is devoid of these advantages shows that it would not be obvious to one of ordinary skill in the art to modify its disclosure to make up for the deficiencies in Yama discussed above. Specifically, if it had been obvious to one of ordinary skill in the art to modify Yama to make up for the deficiencies discussed above, then one of ordinary skill in the art would have done so to attain these advantages. However, no such disclosure have been found that show the claimed invention.

Finally, Japanese Patent A-10112475 does not make up for these deficiencies. In fact, Japanese Patent A-10112475 reinforces the structure and problems of the prior art.

For at least these reasons, it is respectfully submitted that claims 1 and 12 are distinguishable over the applied art. Claims 2-10 and 13-19, and 21-22, which depend from 1 and 12, are likewise distinguishable over the applied art for at least the reasons discussed as well as for the additional features they recite. Withdrawal of the rejections under 35 U.S.C. §102 and §103 is respectfully requested.

III. CONCLUSION

In view of the foregoing remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Kevin M. McKinley
Registration No. 43,794

JAO:KMM/rrs

Attachments:
Appendix
Petition for Extension of Time
Information Disclosure Statement

Date: November 20, 2001

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

Page 12, lines 3-18:

On the surface of the base material of the substrate 10, the film 14 is formed. The film 14 preferably has lower adhesion with the adhesive 30 than with the surface of the base material of the substrate 10. The film 14 is formed to avoid at least one or all of the leads 12. The film 14 is formed so as not to contact at least one or all of the leads 12. Of the plurality of leads 12, not all but at least one may contact the film 14. For example, by contacting leads 12 to be connected to ground potential (GND potential) with the film 14 so as to be electrically conductive, the whole of the film 14 may be at ground potential (GND potential). In this case, since the film 14 which is larger than the leads 12~~14~~ is at ground potential (GND potential), sudden variations in the potential thereof can be absorbed. Also, the potential of the semiconductor chip 20 itself is stabilized.

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Amended) A method of manufacture of a semiconductor device, comprising the steps of:

providing an adhesive between a surface of a semiconductor chip having a plurality of electrodes on which said electrodes are provided and a surface of a substrate having a plurality of leads formed on which said leads are formed;

positioning at least one of said plurality of electrodes to oppose at least one of said plurality of leads; and

applying pressure in a direction such as to make a gap between said semiconductor chip and said substrate narrower;

wherein on the surface of said substrate on which said leads are formed, in a region being at least part of a region of adherence of said semiconductor chip, a film is formed with a lower adhesion to said adhesive than a base material of said substrate, the film formed in such a shape as to avoid the electrodes.

12. (Amended) A semiconductor device comprising:

a semiconductor chip having a plurality of electrodes;

a substrate on which is formed a plurality of leads; and

an adhesive provided between a surface of said semiconductor chip on which said electrodes are formed and a surface of said substrate on which said leads are formed, and adhering said semiconductor chip and said substrate,

wherein at least one of said plurality of electrodes and at least one of said plurality of leads are electrically connected; and

wherein on said substrate in a region including at least a part of a region opposing said semiconductor chip, a film is formed with a lower adhesion to said adhesion than a base material of said substrate, the film formed in such a shape as to avoid the electrodes.